AMENDMENT

To the Claims:

1. (currently amended) A low temperature polysilicon thin film transistor (LTPS-TFT) structure disposed on a substrate, comprising:

a cap layer disposed over the substrate, wherein there is a gap between the cap layer and the substrate;

a polysilicon film disposed over the cap layer, wherein the polysilicon film comprises a channel region and a source/drain region on each side of the channel region, and the channel region is directly above the gap; and

a gate disposed above the channel region of the polysilicon film, wherein the width of the gate is smaller than the average grain size of the channel region, and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate.

2. (original)The LTPS-TFT structure of claim 1, wherein the structure further comprises a buffer layer sandwiched between the substrate and the cap layer so that the gap is disposed between the cap layer and the buffer layer.

3. (original)The LTPS-TFT structure of claim 2, wherein the gap has a coefficient of thermal conductivity smaller than the coefficient of thermal conductivity of the buffer layer.

4. (original)The LTPS-TFT structure of claim 1, wherein the gap has a coefficient of thermal conductivity smaller than the coefficient of thermal conductivity of the substrate layer.

5. (original)The LTPS-TFT structure of claim 1, wherein the structure further comprises a gate dielectric layer disposed over the polysilicon film.

6. (original)The LTPS-TFT structure of claim 1, wherein the grain size of the channel region of the polysilicon film is on average greater than the grain size of the source/drain region of the polysilicon film.

Claim 7. (canceled)

8. (original)The LTPS-TFT structure of claim 1, wherein the gate comprises a dual gate structure.

9. (original)The LTPS-TFT structure of claim 1, wherein the structure further comprises:

a dielectric layer disposed on the polysilicon film and the gate, wherein the dielectric layer has a plurality of contact windows that exposes the source/drain region of the polysilicon film; and

a source/drain conductive layer disposed on the dielectric layer, wherein the source/drain conductive layer is electrically connected to the polysilicon film in the source/drain region through the contact window.

Claims 10-13. (canceled)